REMARKS/ARGUMENTS

In the final Office action dated April 2, 2004, the Examiner allowed claims 22 and 23, indicated claims 5, 7-10, 16 and 18-21 to be allowable if rewritten in independent form and continued to reject all remaining claims (claims 1-4, 6, 11-15 and 17) as obvious over Tran (U.S. Pat. No. 5,875,324) in view of Nair (U.S. Pat. No. 5,890,013). Based on the arguments and amendments contained herein and based on the arguments in Applicants' previous response, Applicants believe all claims to be in condition for allowance.

In amended claim 1, the processor's branch predictor comprises a multi-way branch prediction array "that is used for predictions for conditional branch instructions."[1] Tran does teach a branch prediction array (Figure 2, item 255) and a multi-bank data cache with a "way prediction array" (Figure 52), but Tran does not teach or even suggest a conditional branch prediction array that comprises multiple banks. Figure 52 in Tran relates to a data cache that comprises multiple banks ("ways"). The "way prediction array" shown in Figure 52 is used to predict which way will be "hit" in the data cache's banks. The way prediction array in Tran is not described as being used for the prediction of conditional branch instructions. Applicants have amended claim 1 to clarify that the claimed prediction array is used for predictions for conditional branch instructions. At least for this reason, claim 1 and its dependent claims are allowable.

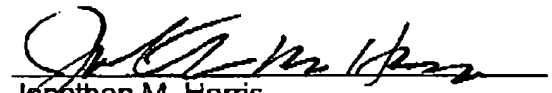
Applicants similarly amended independent claim 12 to specify that the multi-bank branch prediction array is "used to predict conditional branch instructions." As explained above, the art of record does not teach or suggest

[1] As the Examiner no doubt understands, a conditional branch instruction "includes a condition that is checked and the condition can either be true or false. For example, the condition might be to check whether a certain error condition exists. The error condition either exists or not. If the error condition currently exists, the condition is true, otherwise the condition is false (*i.e.*, the condition does not exist). Consequently, one set of instructions is [fetched and] executed if the condition is true, and another set of instructions is [fetched and] executed if the condition is false." Applicants' disclosure, page 2. Thus, the correct prediction of the outcome of conditional branch instructions makes the pipelined nature of a processor operate more efficiently. See page 3. A branch predictor is used to predict the outcome of a conditional branch instruction before the instruction is actually executed so that the correct instructions can be fetched. The Examiner is encouraged to read Applicants' Background section, pages 1-4, for additional information n conditional branch instructions and the usefulness of branch prediction logic.

such a branch prediction array. Accordingly, claim 12 and dependent claims 13-21 are allowable at least for that reason.

Applicants respectfully request that a timely Notice of Allowance be issued in this case. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Respectfully submitted,



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